PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 26 July 2000 (26.07.00)	
International application No. PCT/DK99/00648	**Applicant's or agent's file reference** 23977 PC1
International filing date (day/month/year) 23 November 1999 (23.11.99)	**Priority date** (day/month/year) 24 November 1998 (24.11.98)
Applicant FINSETH, Niels, Christian	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

22 June 2000 (22.06.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer

F. Baechler

Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 23977 PC1	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
International application No. PCT/DK 99/00648	International filing date *(day/month/year)* 23 November 1999	(Earliest) Priority Date *(day/month/year)* 24 November 1998
Applicant GIGA A/S et al		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (See Box I).

2. [ ] **Unity of invention is lacking** (See Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] transcribed by this Authority.

4. With regard to the **title**,
   - [X] the text is approved as submitted by the applicant.
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   - [X] the text is approved as submitted by the applicant.
   - [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:
   Figure No. 2
   - [X] as suggested by the applicant.
   - [ ] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 99/00648

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H04L 7/02
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H04L, H04J, H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 3916084 A (PIERCE C. TOOLE), 28 October 1975 (28.10.75), column 1, line 33 - line 68, figure 2, claims 1-4, abstract --	1-12
Y	EP 0312671 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 26 April 1989 (26.04.89), column 4, line 24 - line 52; column 6, line 4 - line 21, figure 2, claims 1-6, abstract --	1-12
Y	US 5793823 A (SATOSHI NISHIO ET AL), 11 August 1998 (11.08.98), column 2, line 66 - column 3, line 27, figure 2, claims 1-18, abstract	1-4,7-10
A	 --	5,6,11,12

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
2 May 2000

Date of mailing of the international search report
05. 06. 2000

Name and mailing address of the International Searching Authority
European Patent Office P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk
Tel(+31-70)340-2040, Tx 31 651 epo nl.
Fax(+31-70)340-3016

Authorized officer
Klas Arvidsson/cs
Telephone No.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 99/00648

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4339823 A (JOSEPH P. PREDINA ET AL), 13 July 1982 (13.07.82), column 3, line 22 - line 45, figure 4, claims 1,2, abstract	1-4,7-10
A		5,6,11,12
	--	
A	EP 0663744 A1 (FUJITSU LIMITED), 19 July 1995 (19.07.95), column 4, line 18 - column 5, line 15, figures 6,7, claims 1-30, abstract	1-12
	--	
A	US 3851101 A (JOHN EN ET AL), 26 November 1974 (26.11.74), column 1, line 49 - column 2, line 44, claims 1-10, abstract	1-12
	--	
A	GB 2290439 A (OKI ELECTRIC INDUSTRY CO LIMITED), 20 December 1995 (20.12.95), page 5, line 21 - page 6, line 12, figure 1, claims 1-26, abstract	1-12
	--	

INTERNATIONAL SEARCH REPORT
Information on patent family members

02/12/99

International application No.
PCT/DK 99/00648

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3916084 A	28/10/75	NONE	
EP 0312671 A1	26/04/89	CA 1286000 A	09/07/91
		JP 1123544 A	16/05/89
		JP 1913264 C	09/03/95
		JP 6042665 B	01/06/94
		US 4941151 A	10/07/90
US 5793823 A	11/08/98	DE 19537342 A,C	18/04/96
		FR 2725572 A	12/04/96
		JP 8111675 A	30/04/96
US 4339823 A	13/07/82	AU 7377481 A	17/03/82
		CA 1185332 A	09/04/85
		EP 0058166 A	25/08/82
		WO 8200742 A	04/03/82
EP 0663744 A1	19/07/95	CA 2131104 A,C	25/06/95
		JP 7183803 A	21/07/95
		US 5666387 A	09/09/97
US 3851101 A	26/11/74	NONE	
GB 2290439 A	20/12/95	CA 2150767 A	18/12/95
		GB 9511020 D	00/00/00
		HK 1010811 A	00/00/00
		JP 8008988 A	12/01/96
		SG 28292 A	01/04/96
		US 5654987 A	05/08/97

PATENT COOPERATION TREATY

RECD 09 MAR 2001
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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
23977 PC1		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/DK99/00648	23/11/1999	24/11/1998
International Patent Classification (IPC) or national classification and IPC H04L7/00		
Applicant GIGA A/S et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
22/06/2000	05.03.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Bertini, S Telephone No. +49 89 2399 8985

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/DK99/00648

I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-10	as originally filed				

Claims, No.:

1-12	as received on	14/02/2001	with letter of	12/02/2001	

Drawings, sheets:

1/5-5/5	as originally filed				

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-12
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-12
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-12
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

V. REASONED STATEMENT UNDER RULE 66.2(A)(II) WITH REGARD TO NOVELTY, INVENTIVE STEP AND INDUSTRIAL APPLICABILITY

The following documents are cited:

D1:	US 3 916 084	A	(PIERCE C. TOOLE) 28 October 1975
D2:	EP 0 312 671	A1	(INTERNATIONAL BUSINESS MACHINES CORPORATION) 26 April 1989
D3:	US 5 793 823	A	(SATOSHI NISHIO ET AL) 11 August 1998
D4:	US 4 339 823	A	(JOSEPH P. PREDINA ET AL) 13 July 1982
D5:	EP 0 663 744	A1	(FUJITSU LIMITED) 19 July 1995
D6:	US 3 851 101	A	(JOHN EN ET AL) 26 November 1974
D7:	GB 2 290 439	A	(OKI ELECTRIC INDUSTRY CO LIMITED) 20 December 1995
D8:	GB 2 233 177	A	(ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE)

Document D8 has been cited by the Applicant in his reply dated 12.02.2001.

1. It is considered that independent claims 1 (method) and 7 (apparatus) relate to new and inventive subject-matter (Articles 33 (2) and (3) PCT), since the prior art does not disclose or suggest the specifically claimed method for recovering a digital data signal and a clock signal from a received data signal consisting of a number of successive bits according to claim 1 and does not disclose or suggest the specifically corresponding claimed circuit for recovering a digital data signal and a clock signal from a received data signal consisting of a number of successive bits according to claim 7.

   Document D1 is considered to be the closest prior art; document D1 discloses all the features included in the preamble of the independent claims 1 and 7.
   The known system disclosed in D1 however suffers from the drawback of requiring an individual adjustment of every single circuit during production. In particular the delay in the resonance portion of the system may furthermore vary to some extent with the temperature, so that it is not possible to ensure that the

sampling in the flip-flop occurs precisely within the very short time during which the data signal is stable.

Document D2 discloses a predictive clock recovery circuit wherein the duration of the period between two transitions of a multilevel data signal is determined and wherein a pulse signal is generated at half the duration of the said period. A phase locked oscillator driven by the pulse signal generates the extracted clock, the extracted clock being in phase with the generated pulse signal.
In document D2 there is no disclosure of a direct comparison between the phase of the data signal and the resulting phase of the clock signal, being the extracted clock in phase with the pulse signal generated on basis of the data signal. An uncertainty of the position of the clock signal in relation to the centre of the eye intervals of the multilevel data signal is therefore introduced.
In D2 there is no hint of how the data signal is sampled by the clock signal in the centre of the eye opening, i.e. how the data signal is sampled by the recovered clock signal so that the problem of D1 mentioned above is overcome.
D2 furthermore uses a set of counters to obtain a measurement of the duration of the period between two transitions of the multilevel data signal which limits the speed of the overall system since the counters are slow compared to the very high data rates for which the method and the circuit according to the present invention are designed.
Thus, there is in document D1, when taken in combination with document D2, no mention of a method and a corresponding circuit wherein the phase difference between the digital data signal and the recovered clock is measured, and wherein the clock signal is delayed depending on the measured phase difference according to the present invention.

Document D3 discloses a circuit wherein the clock signal is extracted from the data signal and wherein a delay line produces a number of delay clocks. However, document D3 presents the problem that each circuit must be adjusted so as to compensate for the delays introduced in the delay lines.
Document D4 is a clock recovery circuit wherein a transition marker generator produces a pulse signal for each data transition of a multilevel data signal. Again, in D4 the phase error signal is produced by comparing the phase of the pulse signal with the recovered clock signal. There is no direct comparison in D4

between the data signal and the recovered clock signal, with the result that an uncertainty in the implementation of the system is introduced. Furthermore, there is in D4 no mention of how to sample the digital data signal by the recovered clock signal without accounting for the delay introduced by the filter, the PLL and the phase error detector.

Document D8 discloses a digital retiming circuit comprising a phase detector for detecting a phase difference between the incoming data signals and an incoming clock signal which may be extracted from the data signal. D8 discloses a digital phase shifter for shifting the phase of the digital data signal. However, when operating at very high data rates, i.e. where the time periods and the eye opening intervals are very narrow, the digital phase shifter will not be able to relocate the data signal in relation to the clock signal so that the data signal is sampled exactly in the centre of the eye period since the digital sampling is not fast enough in relation to the high bit rates applied with the present invention.

The characterising features of the invention are neither anticipated by the prior art documents D1-D4 and D8 mentioned above nor are rendered obvious by taking into account the disclosure of the other documents cited in the International Search Report.

2. Dependent claims 2 to 6 and 8 to 12 contain further details of the method of claim 1 and of the apparatus of claim 7 respectively. As they are dependent on claims 1 and 7 respectively, they also satisfy the requirements for novelty and inventive step (Articles 33 (2) and (3) PCT).

VII. CERTAIN DEFECTS IN THE INTERNATIONAL APPLICATION

1. The opening part of the description should have been modified to bring it into agreement with any amended independent claims.

2. The prior art documents D1-D4 and D8 should have been acknowledged in the description and the state of the art disclosed therein should have been briefly discussed in the opening part of the description, Rule 5.1 (a) (ii) PCT.

VIII. CERTAIN OBSERVATIONS ON THE INTERNATIONAL APPLICATION (CLARITY)

1. The present wording of the corresponding dependent claims 3 and 9 as well as claims 4 and 10, is not clear (Art. 6 PCT); indeed, the term "at very high data rates" in dependent claims 3 and 9 is vague and relative, and the term "data rates higher than 2.5 GHz" does not correspond to what is indicated in the description on page 1, lines 22-23, as the value 2.5 GHz is also given as an example of the very high data rate, without any further indication concerning "higher" or "lower" than 2.5 GHz.

   Starting from the text of the description on page 1, lines 22-23, a possible wording of a dependent claim 3 (and of a corresponding dependent claim 9) overcoming the raised clarity objection, would include the term "wherein the received data arrives at very high data rates around 2.5 GHz". In such a case the dependent claims 4 and 10 would be superfluous.

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H04L 7/00

A2

(11) International Publication Number: WO 00/31914

(43) International Publication Date: 2 June 2000 (02.06.00)

(21) International Application Number: PCT/DK99/00648

(22) International Filing Date: 23 November 1999 (23.11.99)

(30) Priority Data:
PA 1998 01543 24 November 1998 (24.11.98) DK

(71) Applicant *(for all designated States except US)*: GIGA A/S [DK/DK]; Mileparken 22, DK–2740 Skovlunde (DK).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: FINSETH, Niels, Christian [DK/DK]; Dr. Abildgaards Allé 18, 3.tv, DK–1955 Frederiksberg (DK).

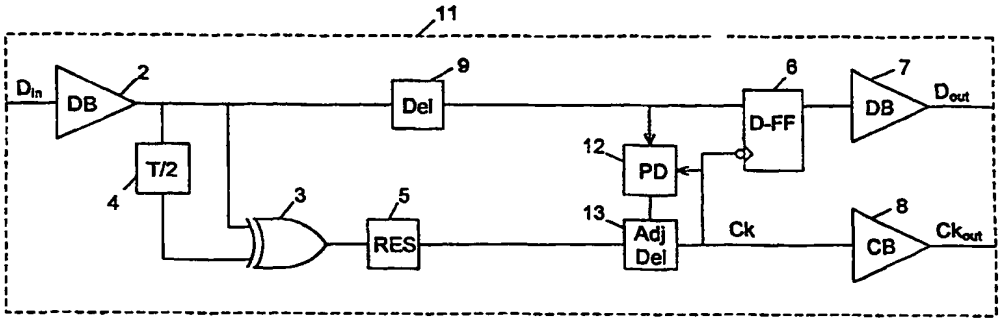
(74) Agent: PLOUGMANN, VINGTOFT & PARTNERS A/S; Sankt Annæ Plads 11, P.O. Box 3007, DK–1021 Copenhagen K (DK).

(81) Designated States: AE, AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), DM, EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KR (Utility model), KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

Without international search report and to be republished upon receipt of that report.

(54) Title: A METHOD AND A CIRCUIT FOR RECOVERING A DIGITAL DATA SIGNAL AND A CLOCK FROM A RECEIVED DATA SIGNAL



(57) Abstract

By application of a method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, a clock signal is produced from the received data signal by means of a resonator circuit (5). The recovered data signal is produced by sampling the received data signal with the recovered clock signal. The received data signal and the recovered clock signal are phase locked to each other so that the received data signal is sampled approximately in the centre of every bit. By phase locking the two signals to each other immediately prior to the sampling, the effect of varying time delays to which the two signals have been subjected individually on their way through the circuit is neutralised, and every sampling may be performed precisely within the very short time during which the data signal is stable.

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Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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A METHOD AND A CIRCUIT FOR RECOVERING A DIGITAL DATA SIGNAL AND A CLOCK FROM A RECEIVED DATA SIGNAL

The invention relates to a method for recovering a digital data signal and a clock signal from a received data signal consisting of a number of successive bits, wherein a clock signal is first produced from the received data signal by means of a resonator circuit, and wherein the recovered data signal is produced by sampling the received data signal with the recovered clock signal. In addition, the invention relates to a corresponding circuit.

When receiving rapid digital data signals in the form of a number of successive bits, e.g. from an optical transmission link, a clock signal will typically be recovered from the received data signal and by means of this clock signal the incoming data will be retimed in e.g. a flip-flop which means that the individual bits of the data signal are synkronized with the clock signal. A number of methods for achieving this are known. In an frequently used method the clock signal is recovered or extracted first by producing a signal having a pulse for each shift in the received data signal and then by filtrating this pulse signal through a resonator circuit. The resonator circuit may e.g. comprise an SAW filter or a dielectric high Q filter. One of the advantages of this method is that a very clean and well defined clock signal is achieved. In addition, the method is well-reputed and verified at very high data rates.

At very high data rates, the individual bit periods are, naturally, very short; the bit period at 2.5 Gbit/s is, e.g., only 400 ps. Hence for every bit the received data signal is stable for only a short period, and it is therefore important that the incoming data signal is sampled quite accurately in the centre of the bit period, or in the centre of the eye diagram as it is also termed. Since the temporal characteristics of both the data signal and the clock signal is subjected to variations originating from the transmission link as well as e.g. process and temperature variations, it is difficult to ensure that the synchronisation between them is sufficient for the sampling actually to be effected in the centre of the bit period.

This may be rectified to some extent by inserting an adjustable time delay element in one of the signals. Typically, the data signal will be delayed since the recovered clock signal is already subjected to some delay in e.g. the resonator circuit. However, this solution requires an adjustment of the circuit in question, and since this adjustment is to be carried out separately for each individual circuit during manufacturing, it is a process that, to a

substantial extent, makes the product more expensive and more complicated. In addition, it is only possible to account for static variations in this manner whereas dynamic variations, which e.g. may be caused by temperature variations, are not accounted for.

Thus, it is an object of the invention to set out a method of the above type, wherein the sampling in the centre of the bit period of the data signal is automatically ensured, and wherein an individual adjustment of the synchronisation in the preceding circuits is thus avoided.

According to the invention this is achieved by phase locking the received data signal and the recovered clock signal to each other in such a manner that the received data signal is sampled approximately in the centre of every bit. By phase locking the two signals to each other immediately before the sampling, the effect of the varying time delays to which the two signals have been subjected on their way through the circuit is neutralised, and every sampling can be performed precisely within the very short time during which the data signal is stable.

As indicated in claim 2, the phase lock may suitably be performed by measuring a phase difference between the recovered clock signal and the received data signal and by time delaying one of them depending on this phase difference.

As indicated in claim 3, it may be the recovered clock signal which is time delayed depending on the measured phase difference. This provides a very exact time adjustment, and in addition it is advantageous that the time delay only has to be implemented at a single frequency since the clock signal only has a single frequency component.

Alternatively, it may, as indicated in claim 4, be the received data signal which is time delayed depending on the measured phase difference.

The time delay may, as indicated in claim 5, be produced by providing the measured phase difference as steering signal to a controllable delay unit. A relatively simple solution is thus obtained in that the desired effect can be achieved with only one component, i.e. a controllable delay unit.

Alternatively, the time delay may, as indicated in claim 6, be produced by providing the measured phase difference as a further steering signal to a frequency locked loop in which a controlled oscillator produces the recovered clock signal controlled by a signal which is produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit. By use of a frequency locked loop for producing the time delayed signal, the latter may generally be produced without jitter, causing the retimed data signal to be largely free of jitter, as well.

As mentioned the invention furthermore relates to a circuit for recovering a digital data signal and a clock signal from a received data signal consisting of a number of successive bits, wherein the circuit comprises a resonator circuit for producing a clock signal from the received data signal and is designed to produce the recovered data signal by sampling the received data signal with the recovered clock signal. As the circuit is designed to phase lock the received data signal and the recovered clock signal to each other so that the received data signal is sampled approximately in the centre of every bit, the effect of the varying time delays to which the two signals have been subjected separately on their way through the circuit is neutralised as described above, and each sampling may be performed precisely within the very short time during which the data signal is stable.

As indicated in claim 8, the circuit may suitably comprise means for measuring a phase difference between the recovered clock signal and the received data signal and for performing said phase lock by time delaying one of them depending on this phase difference.

As indicated in claim 9, it may be the recovered clock signal which is time delayed depending on the measured phase difference by means comprised by the circuit. This provides a very exact time adjustment, and in addition it is advantageous that the time delay only has to be implemented at a single frequency since the clock signal has only a single frequency component.

Alternatively, it may, as indicated in claim 10, be the received data signal which is time delayed by means comprised by the circuit depending on the measured phase difference.

The circuit may, as indicated in claim 11, comprise a controllable delay unit for producing said time delay controlled by the measured phase difference. A relatively simple solution

is thus obtained in that the desired effect can be achieved with only one component, i.e. a controllable delay unit.

Alternatively, the circuit may, as indicated in claim 12, comprise af frequency locked loop for producing said time delay, in which loop a controlled oscillator may produce the recovered clock signal controlled by a signal which is produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit, the frequency locked loop in addition being designed to produce said time delay by application of the measured phase difference as a further steering signal to said loop. By use of a frequency locked loop for producing the time delayed signal, the latter may generally be produced without jitter, causing the retimed data signal to be largely free of jitter, as well.

The invention will be described in greater detail below with reference to the drawings in which:

Fig. 1 shows a known circuit for recovering a digital data signal and a clock signal from a received data signal,

Fig. 2 shows a first embodiment of a circuit according to the invention,

Fig. 3 shows an example of the structure of a phase detector for use in the circuit of Fig. 2,

Fig. 4 shows a second embodiment of a circuit according to the invention, and

Fig. 5 shows a third embodiment of a circuit according to the invention.

The disclosed circuits hereunder are preferably integrated on a single or several integrated circuits. To support the required high-speed operation of the present circuits, logic gates and circuit blocks are preferably implemented as CML logic using bipolar transistors. The preferred process is a 2.0 μm Bipolar process suitable digital circuits operating within the frequency range of about 622 MHz to 10 GHz. The NPN transistors provided by this process have f_T values of about 25 GHz. Alternatively, commercially available 0.13 - 0.25 μm CMOS processes with sufficiently fast transistors may be

capable of being applied in some applications of the present invention, at least for circuits operating at the lower system frequencies.

Fig. 1 shows an otherwise known circuit 1 to which the invention may be applied. The circuit shown is a part of a receiver circuit which may receive a digital data signal e.g. from an optical transmission link. Only the data signal itself is transmitted in the optical transmission link and consequently a matching clock signal therefore has to be extracted in the receiver from the received data signal. The incoming data signal D_{in} is led to an XOR circuit 3 via a data buffer 2, partly directly and partly via a delay element 4. If the signal D_{in} is constituted by a data stream of e.g. 2.5 Gbit/s, the bit period T will be 400 ps, and the delay of the delay element 4 may then be T/2 or 200 ps. At the output of the XOR circuit 3 a pulse signal with a pulse of 200 ps will occur for each shift in the data signal. This pulse signal is led to the input of a resonator circuit 5 which e.g. may be a SAW filter or a dielectric high Q filter. The circuit 1 itself will typically be formed as an integrated circuit and the resonance circuit 5 may then optionally be an external component which is coupled to the integrated circuit.

Since the resonance circuit 5 has a very high Q, a stable clock signal Ck of 2.5 GHz will appear at its output, and this clock signal may then be used for sampling the data signal D_{in} in a flip-flop 6 so that a retimed data signal D_{out} , i.e. a data signal which is synchronised with the recovered clock signal Ck, will appear at the output of the circuit (via a data buffer 7). Via a clock signal buffer 8 the recovered clock signal is also available as the signal Ck_{out} at the output of the circuit, said clock signal also being used in following circuits. A delay element 9 is inserted in the transmission path of the received data signal D_{in} from the buffer 2 to the flip-flop 6 for the purpose of compensating for the delay to which the clock signal is inevitably subjected in e.g. the XOR circuit 3 and the resonator circuit 5 so that the sampling in the flip-flop 6 occurs approximately in the centre of the bit period of the data signal.

The delay element 9 may optionally be adjustable to compensate for production tolerances; however, this requires an individual adjustment of every single circuit during production which to a substantial extent makes the product more expensive and more complicated. Since especially the delay in the resonator circuit 5 may furthermore vary to some extent with the temperature, the delay element 9 at the very high data rates, i.e. the

very short bit periods, is, however, not able to ensure that the sampling in the flip-flop 6 occurs precisely within the very short time during which the data signal is stable.

Fig. 2 thus shows a circuit 11 according to the invention wherein this problem is solved. The largest part of the circuit 11 corresponds to the circuit 1 of Fig. 1 and components which are included in both figures also designate the same reference numbers. A phase detector 12, the operation of which will be described in greater detail below, compares the recovered clock signal Ck with the data signal and produces a signal at its output, expressing the phase difference between the two signals and thus between the optimum sampling time and the actual sampling time. The output signal from the resonator circuit 5 is not used directly as the recovered clock signal but is instead led to the input of a controllable delay unit 13 controlled by the output signal from the phase detector 12. The output signal from the delay unit 13 then constitutes the recovered clock signal Ck which has been adjusted now to obtain the optimum sampling time in the flip-flop 6. The circuit 11 also shows a delay unit 9 in the data signal path. The latter may still be appropriate to compensate for the greater delay of the clock signal in the circuit 3 and the resonator circuit 5 since the controllable delay element 13, naturally, provides only positive delays. It should be noted that the delay unit 13 may also in principle consist of a fixed and a controllable delay.

Fig. 3 shows an example of the structure of the phase detector 12. As mentioned above, the phase detector 12 compares the recovered clock signal Ck with the data signal D_{in} and produces a signal at its output, said signal being a measure of the phase difference between the two signals, and thus between the optimum sampling time and the actual sampling time. This is effected by the recovered clock signal Ck being used for sampling the data signal D_{in} in three flip-flops 21, 22, 23 at three different points in time. If the type of flip-flop applied is designed to sample on a positive clock signal edge, the outputs of the two flip-flops 21 and 22 will show the present and preceding sampling value of the data signal, respectively. The present value is called sample C (SC), whereas the preceding value is called sample A (SA). The delay in flip-flop 21 is taken to be sufficient for a new sampling value at the output (SC) caused by a positive clock signal edge not to appear until after flip-flop 22 has performed its sampling caused by said clock signal edge. If this is not the case, an additional delay element between the two flip-flops has to be inserted.

Due to the inverter 24, flip-flop 23 will sample the data signal on the negative edge of the clock signal resulting in a sampling value (sample B, SB) in between the two others, i.e. about that time when the transistion from the preceding to the present bit period occurs, the posititive and negative half periods of the clock signal being taken to be of equal length. If this is not the case, the inverter 24 may be replaced by a delay circuit with a delay corresponding to half a clock signal period.

Thus, at the outputs of the three flip-flops, three successive sampling values will be represented, i.e. SA which was performed approximately in the centre of the preceding bit period, SB which was performed about the time when the transition from the preceding to the present bit period occurs, and SC which was performed approximately in the centre of the present bit period. A signal SAC is produced by means of an XOR circuit 25 and a subsequent inverter 26, said signal being, logically, "1" if the sampling values SA and SC are identical, and being, logically, "0" if they are different, i.e. there has been a shift from the preceding to the present bit period. Similarly, a signal SAB is produced by means of an XOR circuit 27 and a subsequent inverter 28, said signal being, logically, "1" if the sampling values SA and SB are identical, and being, logically, "0" if they are different.

Subsequently, two NOR circuits 29 and 30 produce two signals, UP and DOWN. If SAC is logically "1", corresponding to the sampling values SA and SC being identical, both signals, UP and DOWN, will logically be "0" irrespective of the value of SAB, the sampling value SB being insignificant, since it is impossible, in this situation, to extract information about the position of the sampling time.

If, on the other hand, SAC is logically "0", corresponding to a shift from the preceding to the present bit period having taken place, the signals, UP and DOWN, are determined by the signal SAB. The signal DOWN will logically be "1" if SAB is "1" corresponding to sampling values SA and SB being identical as a result of the shift from the preceding to the present bit period having taken place later than the negative edge of the clock signal. In that case the clock signal is too early compared to the optimum sampling time and the signal DOWN signals that it has to be further delayed. If, on the other hand, SAB is "0", the signal UP will logically be "1", corresponding to the sampling values SA and SB being different as a result of the shift from the preceding to the present bit period having taken place prior to the negative edge of the clock signal. In that case the clock signal is too late

compared to the optimum sampling time and the signal UP signals that the delay has to be reduced.

In order to convert the two signals UP and DOWN to a single signal which is led via the filter 12 to the delay element 13, the two signals are led to a tristate circuit or a charge pump 31. When both signals are "0", the output of the circuit 31 is in a state of high impedance (tri-state) so that the delay element 13 is not affected, i.e. the delay is not changed. When the signal UP is, logically, "1", the circuit 31 provides a positive charging current which is led to the delay element 13 and thus increases the control voltage so that the delay is reduced. Similarly, when the signal DOWN is, logically, "1", the circuit 31 provides a negative charging current which is led to the delay element 13 and thus reduces the control voltage so that the delay is increased. Thus, the clock signal Ck will be adjusted continuously in order that sampling B is always performed precisely at the transition time and consequently sampling C in the centre of the bit period.

Further, it should be noted that in the shown circuit the two flip-flops 6 and 21 perform the same function, the signal SC at the output of the flip-flop 21 being identical to the signal constituting the retimed data signal D_{out} at the output of the flip-flop 6. One of the two flip-flops may thus be omitted. When two separate flip-flops are mentioned above it is for the purpose of clearness only.

In fig. 2 the controllable delay unit 13 is inserted in the clock signal branch in order that the recovered clock signal is delayed depending on the phase difference measured by the phase detector 12. The crucial point of the invention is, however, simply that the clock signal and the data signal are adjusted with respect to each other whereas it is not crucial whether the clock signal or the data signal is subjected to the variable delay. Thus, in Fig. 4 is shown an alternative embodiment of a circuit 33 according to the invention. Instead of the controllable delay unit 13 in the clock signal branch a controllable delay unit 34 is inserted in the data signal branch. Here, the phase detector 12 compares the recovered clock signal Ck with the delayed data signal and produces, as previously, a signal at its output, said signal being a measure of the phase difference between the two signals, and thus between the optimum sampling time and the actual sampling time. The other parts of the circuit in Fig. 4 are unchanged compared to the circuit in Fig. 2. Further, it should be noted that the fixed delay 9 and the controllable delay unit 34 may optionally be combined in one single unit.

In Figs. 2 and 4 the clock signal and the data signal, respectively, are delayed by means of a controllable delay units 12 and 34, respectively. Fig. 5 shows an embodiment wherein the delay is produced in another manner. The recovered clock signal Ck is here produced by a voltage-controlled oscillator 37 which is frequency locked to the output signal of the resonator circuit 5. The clock signal Ck is led back to a phase frequency detector 35 to be compared with the output signal from the resonator circuit 5. Any frequency difference between the two clock signals will result in an error signal at the output of the phase frequency detector 35, said signal being fed to the voltage-controlled oscillator 37 as a steering signal via a low-pass filter 36.

This contributes to ensuring that the recovered clock signal Ck is frequency locked to the output signal from the resonator circuit 5. However, it does not ensure that the sampling of the data signal in the flip-flop 6 is performed at the appropriate point in time in relation to the data signal. This is achieved when the phase detector 12 compares the recovered clock signal Ck with the data signal and produces a signal at its output, said signal being a measure of the phase difference between the two signals, and thus between the optimum sampling time and the actual sampling time. This offset signal is filtered in the low-pass filter 38 and is then added in the summing point 39 to the error signal from the phase frequency detector 35 before the error signal is fed to the low-pass filter 36 in the original loop. This results in a phase change of the voltage-controlled oscillator 37, and thus of the recovered clock signal. If the time constants for the two filters 36 and 38 are selected so that the low-pass filter 38 is much slower than the low-pass filter 36, the loop consisting of the phase detector 12, the low-pass filters 38 and 36 and the voltage-controlled oscillator 37 will adjust the recovered clock signal Ck to obtain the optimum sampling time in the flip-flop 6. The other parts of the circuit in Fig. 5 are unchanged compared to the circuit in Fig. 2.

For a circuit 11 adapted to operate in the 2.5 GHz range, a time-constant for the low-pass filter 38 of about 100 μS, corresponding to a cut-off frequency of about 10 kHz, such as between 1 KHz and 50 kHz is preferred. As explained above, the time constant of low-pass filter 36 is preferably selected to be significantly smaller the time constant of filter 38, i.e. low-pass filter 36 has, preferably, a substantially higher cut-off frequency than the cut-off frequency of low-pass filter 38. Preferably, the cut-off frequency of low-pass filter 36 is selected as being about 10 - 20 times higher than the cut-off frequency of low-pass filter 38. Accordingly, for operation in the 2.5 GHz range and a selected cut-off frequency of

about 10 kHz in low-pass filter 38, a cut-off frequency of about 100 kHz, such as between 40 kHz and 2 MHz should be selected for low-pass filter 36. For higher or lower system operating frequencies, e.g. 10 GHz or 622 MHz (corresponding to STM 64 and STM 4, respectively), these cut-off frequencies are preferably scaled substantially proportionally.

It should be noted that the method of Fig. 5 for production of the time difference may also be applied when the data signal is delayed as in Fig. 4.

Even though preferred embodiments of the present invention have been described and shown, the invention is not limited thereto, but may also be implemented according to other embodiments within the scope of the following claims.

CLAIMS:

1. A method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, wherein a clock signal is first produced from the received data signal by means of a resonator circuit (5), and wherein the recovered data signal is produced by sampling the received data signal with the recovered clock signal,
characterised in that the received data signal and the recovered clock signal are phase locked to each other so that the received data signal is sampled approximately in the centre of every bit.

2. A method according to claim 1, characterised in that said phase lock is performed by measuring a phase difference between the recovered clock signal and the received data signal and by time delaying one of them depending on this phase difference.

3. A method accoding to claim 1 or 2, characterised in that the recovered clock signal is time delayed depending on the measured phase difference.

4. A method accoding to claim 1 or 2, characterised in that the received data signal is time delayed depending on the measured phase difference.

5. A method according to claims 2-4, characterised in that said time delay is produced by applying the measured phase difference as steering signal to a controllable delay unit (13; 34).

6. A method according to claims 2-4, characterised in that said time delay is produced by providing the measured phase difference as a further steering signal to a frequency locked loop, wherein a controlled oscillator (37) produces the recovered clock signal controlled by a signal, said signal being produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit.

7. A circuit for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, wherein the circuit comprises a resonator circuit (5) for producing a clock signal from the received data signal

and is designed to produce the recovered data signal by sampling the received data signal with the recovered clock signal,
characterised in that it is designed to phase lock the the received data signal and the recovered clock signal to each other so that the received data signal is sampled approximately in the centre of every bit.

8. A circuit according to claim 7, characterised in that it comprises means (12) for measuring a phase difference between the recovered clock signal and the received data signal and for performing said phase lock by time delaying one of them depending on this phase difference.

9. A circuit according to claim 7 or 8, characterised in that it comprises means (13; 35, 36, 37, 38 ,39) for time delaying the recovered clock signal depending on the measured phase difference.

10. A circuit according to claim 7 or 8, characterised in that it comprises means (34) for time delaying the received data signal depending on the measured phase difference.

11. A circuit according to claims 8-10, characterised in that it comprises a controllable delay unit (13; 34) designed to produce said time delay controlled by the measured phase difference.

12. A circuit according to claims 8-10, characterised in that it comprises a frequency locked loop, wherein a controlled oscillator (37) may produce the recovered clock signal controlled by a signal, said signal being produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit (5), and wherein the frequency locked loop is furthermore designed to produce said time delay by provision of the measured phase difference as a further steering signal to said loop.

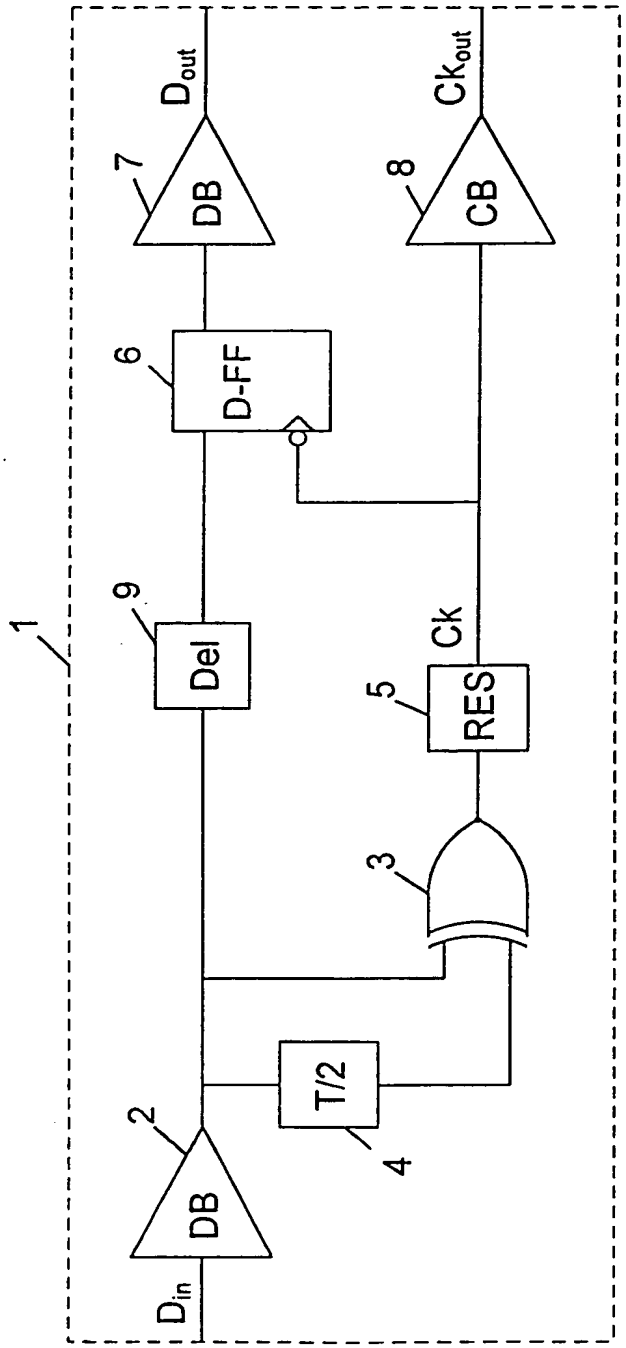
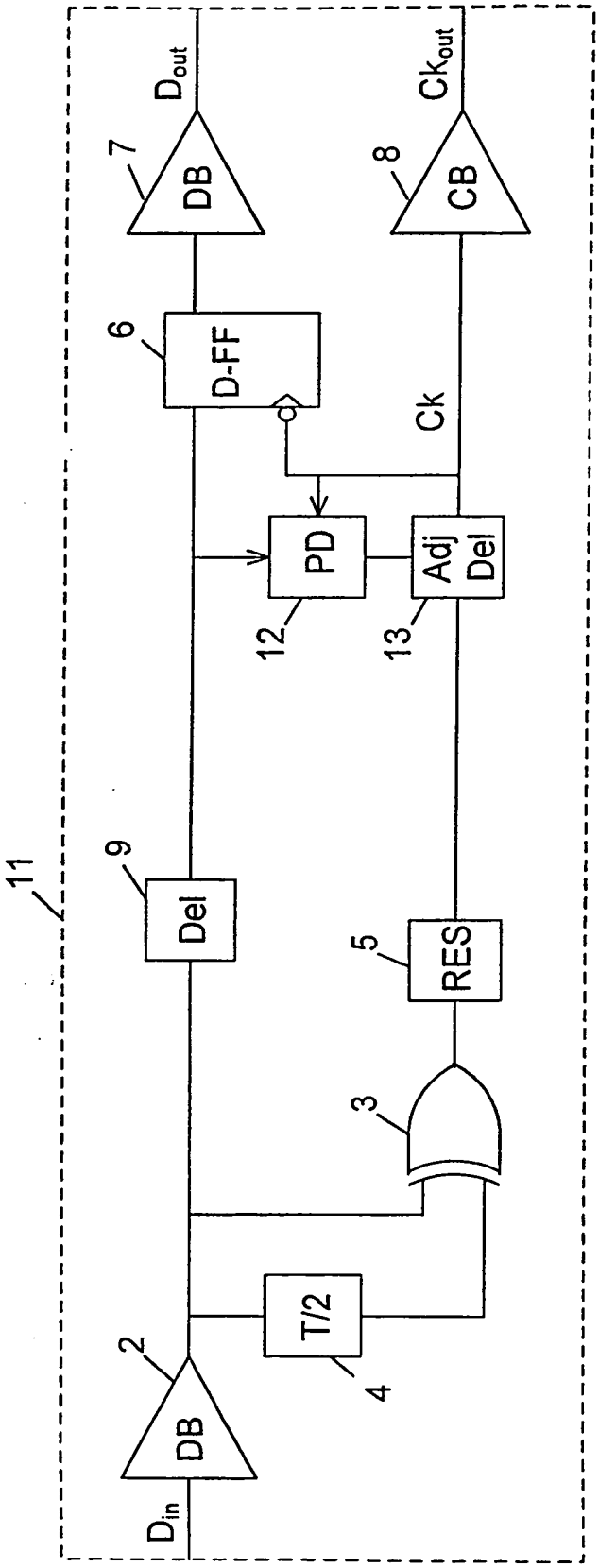


Fig. 1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Ck_{out}
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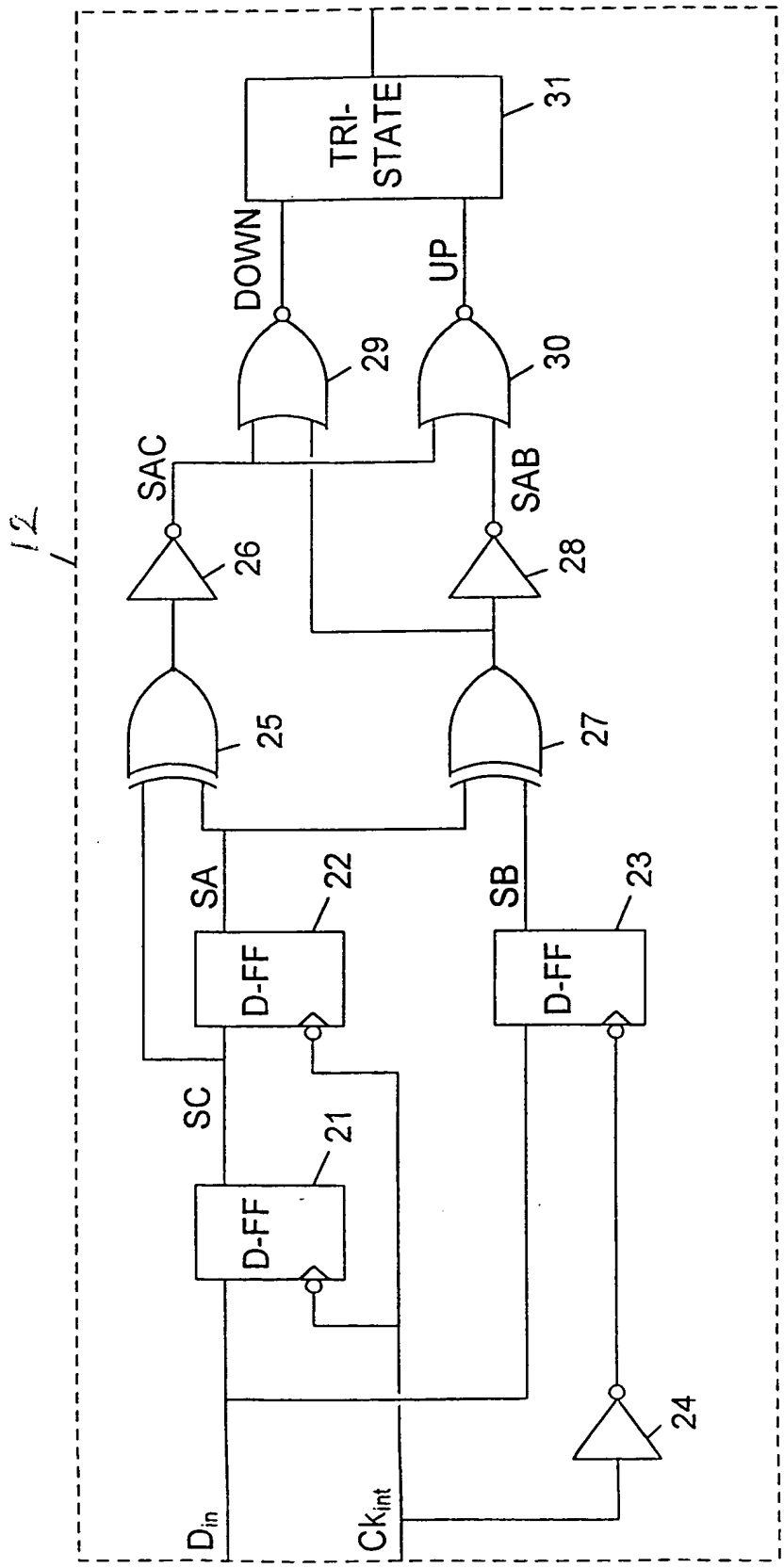
DB
8
CB
6
D-FF
Ck
PD
Adj Del
12
13
11
9
Del
5
RES
3
T/2
4
2
DB
D_{in}

Fig. 2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UP
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30
SAC
SAB
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28
25
27
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SB
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SC
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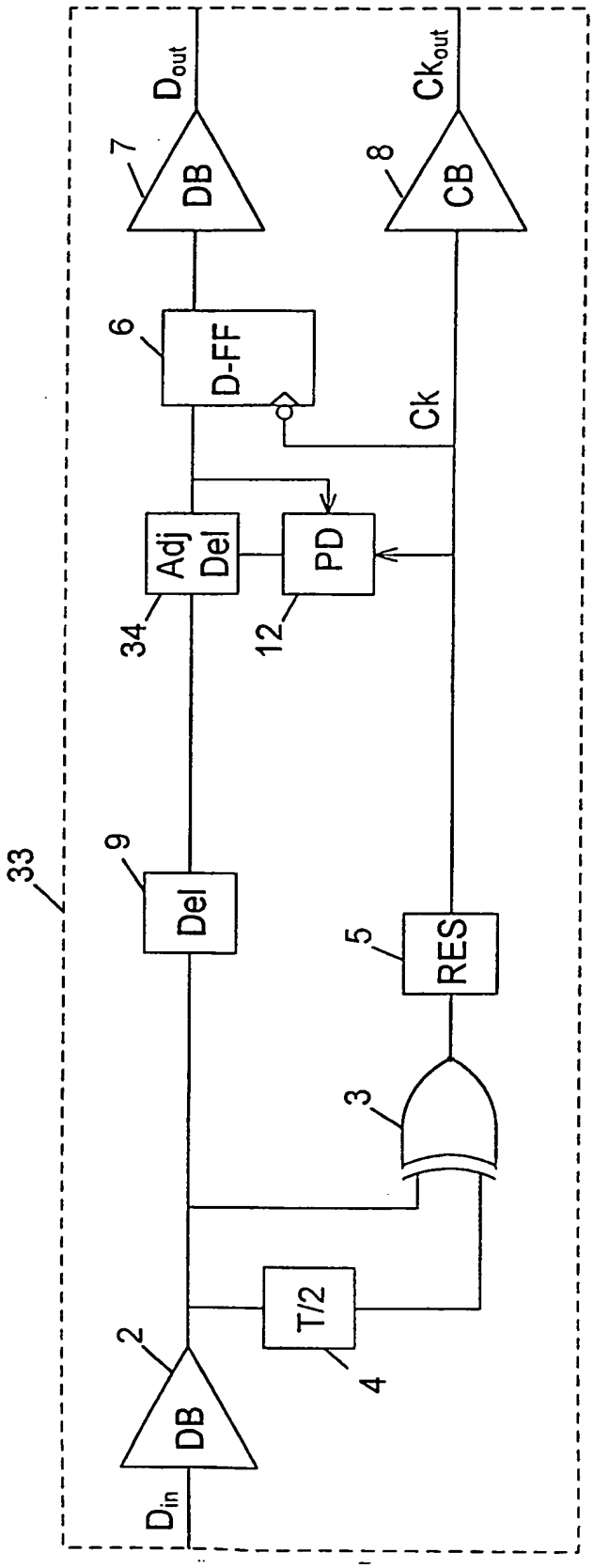
D-FF
24
D_{in}
Ck_{int}

Fig. 3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6
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Ck
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RES
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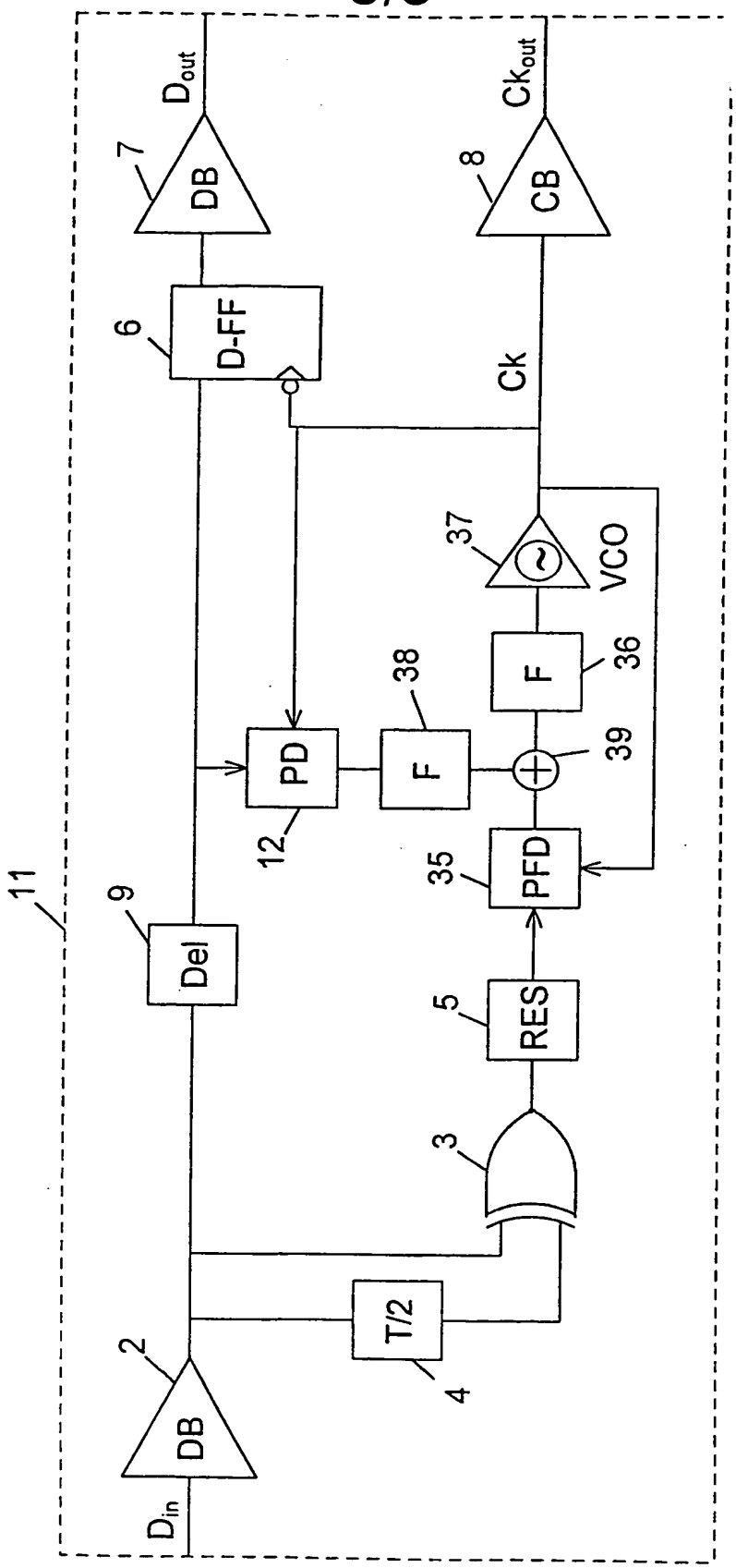
T/2
4
2
DB
D_{in}

Fig. 4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36
38
F
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35
PFD
11
9
Del
5
RES
3
T/2
4
2
DB
D_{in}

Fig. 5

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(71) Applicant *(for all designated States except US)*: GIGA A/S [DK/DK]; Mileparken 22, DK–2740 Skovlunde (DK).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: FINSETH, Niels, Christian [DK/DK]; Dr. Abildgaards Allé 18, 3.tv, DK–1955 Frederiksberg (DK).

(74) Agent: PLOUGMANN, VINGTOFT & PARTNERS A/S; Sankt Annæ Plads 11, P.O. Box 3007, DK–1021 Copenhagen K (DK).

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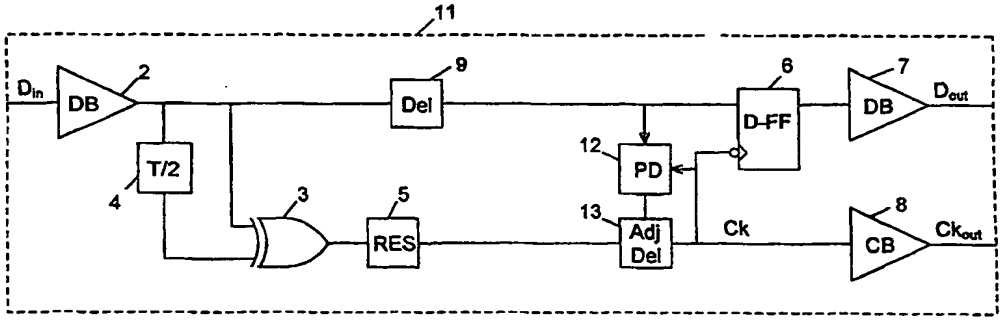

(57) Abstract

By application of a method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, a clock signal is produced from the received data signal by means of a resonator circuit (5). The recovered data signal is produced by sampling the received data signal with the recovered clock signal. The received data signal and the recovered clock signal are phase locked to each other so that the received data signal is sampled approximately in the centre of every bit. By phase locking the two signals to each other immediately prior to the sampling, the effect of varying time delays to which the two signals have been subjected individually on their way through the circuit is neutralised, and every sampling may be performed precisely within the very short time during which the data signal is stable.

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 3916084 A (PIERCE C. TOOLE), 28 October 1975 (28.10.75), column 1, line 33 - line 68, figure 2, claims 1-4, abstract --	1-12
Y	EP 0312671 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 26 April 1989 (26.04.89), column 4, line 24 - line 52; column 6, line 4 - line 21, figure 2, claims 1-6, abstract --	1-12
Y	US 5793823 A (SATOSHI NISHIO ET AL), 11 August 1998 (11.08.98), column 2, line 66 - column 3, line 27, figure 2, claims 1-18, abstract	1-4,7-10
A	 --	5,6,11,12

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the International Searching Authority European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel(+31-70)340-2040. Tx 31 651 epo nl. Fax(+31-70)340-3016	Authorized officer Klas Arvidsson/cs Telephone No.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 99/00648

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4339823 A (JOSEPH P. PREDINA ET AL), 13 July 1982 (13.07.82), column 3, line 22 - line 45, figure 4, claims 1,2, abstract	1-4,7-10
A		5,6,11,12
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A	EP 0663744 A1 (FUJITSU LIMITED), 19 July 1995 (19.07.95), column 4, line 18 - column 5, line 15, figures 6,7, claims 1-30, abstract	1-12
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A	US 3851101 A (JOHN EN ET AL), 26 November 1974 (26.11.74), column 1, line 49 - column 2, line 44, claims 1-10, abstract	1-12
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A	GB 2290439 A (OKI ELECTRIC INDUSTRY CO LIMITED), 20 December 1995 (20.12.95), page 5, line 21 - page 6, line 12, figure 1, claims 1-26, abstract	1-12
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INTERNATIONAL SEARCH REPORT

Information on patent family members

02/12/99

International application No.
PCT/DK 99/00648

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Tyskland

PCT CHAPTER II

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12 February 2001

International Patent Application No. PCT/DK99/00648
Publication No. WO 00/31914
GIGA
Our ref: 23977 PC 1

COPENHAGEN OFFICE:
SANKT ANNÆ PLADS 11
POST OFFICE BOX 3007
DK - 1021 COPENHAGEN K
A.S REG. NO. 223795
TELEPHONE +45 33 63 93 00
TELEFAX +45 33 63 96 00
e-mail pv@pv.dk
www.pv.dk

Artist Bjørn Bjørnholt

AARHUS OFFICE:
NOBELPARKEN
JENS CHR. SKOUS VEJ 9
POST OFFICE BOX 49
DK - 8100 AARHUS C
TELEPHONE +45 87 39 18 00
TELEFAX +45 33 63 96 00
e-mail pv@pv.dk
www.pv.dk

Dear Sirs,

Referring to the written opinion dated 27 October 2000, we hereby submit a set of amended claims 1-12 in replacement of all claims 1-12 currently on file, wherein

- Claim 1 has been amended to include the features of previous claims 2 and 3 (now deleted),
- Previous claim 4 has been deleted,
- New claim 2 corresponds to previous claim 5,
- Claims 3 and 4 are new, basis for the new claims is found in the description on page 1, line 21-23,
- Basis for new claim 5 is found in the description on page 4, lines 32-33,
- The features of new claim 6 correspond to the features of previous claim 6,
- New claim 7 corresponds to previous claim 7 amended to include the features of previous claims 8 and 9 (now deleted),
- Previous claim 10 has been deleted,
- New claim 8 corresponds to previous claim 11,
- Claims 9 and 10 are new and basis for the new claims is found in the description on page 1, lines 21-23,
- Basis for new claim 11 is found in the description on page 4, lines 32-33,

- The features of new claim 12 correspond to the features of previous claim 12.

Document D1 discloses a system for recovering a digital data signal and a clock signal from a received data signal. The clock signal is produced from the digital data signal via a resonator circuit and the recovered data signal is produced by sampling the received data signal with the recovered clock signal. Applicant agrees with the Examiner that the document D1 discloses what is described in the preamble of claim 1.

Document D2 discloses a predictive clock recovery circuit wherein the duration of the period between two transitions of a multilevel data signal is determined and wherein a pulse signal is generated at half the duration of the said period. A phase locked oscillator driven by the pulse signal generates the extracted clock, the extracted clock being in phase with the generated pulse signal.

The extracted clock signal in D2 is, thus, in phase with the pulse signal generated on basis of the data signal. There is no direct comparison between the phase of the data signal and the resulting phase of the clock signal, whereby an uncertainty of the position of the clock signal in relation to the centre of the eye intervals of the multilevel data signal is introduced.

Furthermore, in D2, a set of counters is used to obtain a measurement of the duration of the period between two transitions of the multilevel data signal. The use of counters limit the speed of the overall system since the counters are slow compared to the very high data rates for which the method and the circuit according to the present invention are designed.

Furthermore, applicant finds it unclear how the data signal is sampled by the clock signal in the centre of the eye opening. There is throughout the description no mentioning of how the data signal is sampled by the recovered clock signal so that the problem of D1, i.e. the problem of introducing a delay between the recovered clock signal and the data signal due to the counters, is overcome.

Thus, there is in document D1, when taken in combination with D2, no mentioning of a method and a corresponding circuit wherein the phase difference between the digital data signal and the recovered clock is measured, and wherein the clock signal is delayed depending on the measured phase difference according to the present invention.

Document D3 discloses a circuit wherein the clock signal is extracted from the data signal and wherein a delay line (1) produces a number of delay clocks. A delay clock having its rise almost corresponding to that of an external data signal is the clock selected. The data signal is then delayed in the elastic store circuit (7) so that the output of the elastic store circuit, the internal data signal, is in synchronisation with the internal clock. The problem of D3 is again that each circuit must be adjusted so as to compensate for the delays introduced in the delay lines.

Document D4 is a clock recovery circuit wherein a transition marker generator produces a pulse signal for each data transition of a multilevel data signal. The pulse signal is then provided to a tunable bandpass filter wherein the pulse signal is

filtered so that an approximately sinusoidal signal is generated at the output of the filter. The bandpass filter furthermore shifts the phase of the pulse signal according to a phase error signal. The output of the filter is provided to a PLL producing the recovered clock signal, and the phase error signal is produced by comparing the phase of the pulse signal with the recovered clock signal. Again, there is no direct comparison between the data signal and the recovered clock signal, thus an uncertainty in the implementation of the system is introduced.

Furthermore, there is in D4 no mentioning of how to sample the digital data signal by the recovered clock signal without accounting for the delay introduced by the filter, the PLL and the phase error detector.

The attention of the Examiner is furthermore drawn to British Patent Appl. No. GB 2 233 177. GB 2 233 177 discloses a digital retiming circuit comprising a phase detector for detecting a phase difference between the incoming data signals and an incoming clock signal which may be extracted from the data signal (cf. page 1).The output signals from the phase detector are provided to a phase shifter U2 which is a digital loop processor generating a control bus signal based on the output of the phase detector.

The control bus signal is then provided to a phase shifter U3 controlling the phase of the input data according to the control bus signal.

GB 2 233 177, thus, discloses a digital phase shifter for shifting the phase of the digital data signal. However, when operating at very high data rates, i.e. where the time periods and the eye opening intervals are very narrow, the digital phase shifter will not be able to relocate the data signal in relation to the clock signal so that the data signal is sampled exactly in the centre of the eye period since the digital sampling is not fast enough in relation to the high bit rates applied with the present invention.

Furthermore, application of an analogue phase shifter instead of the digital phase shifter in order to provide a continuous variability of the phase of the digital data signal is briefly discussed in the preamble of the description, cf. page 2, and found to have too many disadvantages. Still further, the task of implementing an analogue phase shifter, such as a controllable delay, in the data signal is a cumbersome task due to the large amount of frequencies present in the data signal wherefore the digital phase shifter is chosen.

Applicant finds that none of the mentioned documents either when taken alone or in combination discloses a method and a circuit for recovering a digital data signal and a clock signal according to the present invention, wherein the data signal and the recovered clock signal are phase locked to each other, the phase lock being performed by measuring a phase difference between the recovered clock signal and the data signal and delaying the clock signal according to the phase difference so that the received data signal is sampled approximately in the centre of every bit.

In respect of the above-mentioned, applicant finds that the subject-matter of new independent claims 1 and 7 fulfils the requirements of Art. 33(3) PCT.

The Applicant wishes to defer any amendments of the description and remedy of formal deficiencies until the Examiner has indicated that the new claims have been found allowable.

In case the Examiner does not agree that the new claims are properly based on the documents originally filed, and that the invention defined in the new claims is novel and involves an inventive step, a personal interview with the Examiner pursuant to Rule 66.6 PCT is requested prior to the issuance of a preliminary examination report.

Please acknowledge receipt of this letter by means of the enclosed form 1037.

Yours sincerely,

Plougmann, Vingtoft & Partners

CRN

Camilla Rendal Nielsen

GB 2 233 177 (by mail only)
New claims 1-12 (in triplicate by mail only)
Form 1037

International Patent Application No. PCT/DK99/00648
GIGA A/S
Our ref. 23977 PC1

CLAIMS:

1. A method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, wherein a clock signal is first produced from the received data signal by means of a resonator circuit (5), and wherein the recovered data signal is produced by sampling the received data signal with the recovered clock signal, characterised in that the received data signal and the recovered clock signal are phase locked to each other by measuring a phase difference between the recovered clock signal and the received data signal and by time delaying the recovered clock signal depending on this phase difference, so that the received data signal is sampled approximately in the centre of every bit.

2. A method according to claim 1, wherein said time delay is produced by applying the measured phase difference as steering signal to a controllable delay unit (13; 34),

3. A method according to claim 1 or 2, wherein the received data arrives at very high data rates.

4. A method according to claim 3, wherein the data rates are higher than 2.5 GHz.

5. A method according to claims 1 or 2, the method being operated at frequencies between 622 MHz and 10 GHz.

6. A method according to claim 1, characterised in that said time delay is produced by providing the measured phase difference as a further steering signal to a frequency locked loop, wherein a controlled oscillator (37) produces the recovered clock signal controlled by a signal, said signal being produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit.

7 A circuit for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) from a received data signal (D_{in}) consisting of a number of successive bits, wherein the circuit comprises a resonator circuit (5) for producing a clock signal from the received data signal and is designed to produce the recovered data signal by sampling the received data signal with the recovered clock signal, characterised in that it comprises means (12) for measuring a phase difference between the recovered clock signal and the received data signal and for phase locking the recovered clock signal and the received data signal by time delaying the recovered clock signal depending on this phase difference, the circuit further comprises means (13; 35, 36, 37, 38 ,39) for time delaying the recovered clock signal depending on the measured phase difference so that the received data signal is sampled approximately in the centre of every bit.

8. A circuit according to claim 7, characterised in that it comprises a controllable delay unit (13; 34) designed to produce said time delay controlled by the measured phase difference.

9. A circuit according to claim 7 or 8, adapted to receive data arrives at very high data rates.

10. A circuit according to claim 9, wherein the circuit is adapted to receive data at data rates higher than 2.5 GHz.

11. A circuit according to any of claims 7-10, wherein the circuit is adapted to be operated at a frequency between 622MHz and 10 GHz.

12. A circuit according to claim 7, characterised in that it comprises a frequency locked loop, wherein a controlled oscillator (37) may produce the recovered clock signal controlled by a signal, said signal being produced as a measure of a frequency variation between the recovered clock signal and an output signal from said resonator circuit (5), and wherein the frequency locked loop is furthermore designed to produce said time delay by provision of the measured phase difference as a further steering signal to said loop.